REMARKS

Claims 1, 2, 4, and 6-8 are now present in this application.

Claims 3 and 5 have been cancelled, claim 1 has been amended, and claims 6-8 have been added. Reconsideration of the application, as amended, is respectfully requested.

The drawings stand objected to for an informality. In view of the foregoing amendments to the drawings, it is respectfully submitted that these informalities have been addressed. Reconsideration and withdrawal of any objection to the drawings are respectfully requested.

The disclosure stands objected to for various informalities. In view of the foregoing amendments, it is respectfully submitted that these informalities have been addressed. Reconsideration and withdrawal of any objection to the disclosure are respectfully requested.

Claims 4-5 stand rejected under 35 USC 112, first paragraph. This rejection is respectfully traversed.

With regard to the 35 USC 112, first paragraph rejection, the Examiner has asserted that there is no explanation of how to offset flicker and display brightness or to use STV 1 signal to determine a start scan location of a frame. It is noted that, on page 2, lines 19-24 of the present specification, the prior art discloses the start vertical signals STV including a first start vertical

signal STV for determining a start scan location of a frame, and a second start vertical signal STV2, for offsetting the flicker and brightness display. Thus, how to offset flicker and display brightness should be reasonably understood by one skilled in the art. Accordingly, reconsideration and withdrawal of the 35 USC 112, first paragraph rejection are respectfully requested.

Claims 1-5 stand rejected under 35 USC 102(b) as being anticipated by the Applicants' admitted prior art.

It is respectfully submitted that the Applicants' admitted prior art teaches a next control signal generated according to a memory value of a previous horizontal or vertical cycle. When an LCD module is in DE mode or in the mode of three synchronizing signals HSYNC, VSYNC, DE, the timing controller processes signals according to the memory values of horizontal and vertical cycles, such as the vertical blank period VB (v-blank) and the gate clock signal CPV. For example, in a vertical blank period VB (v-blank) of the data enable signal DE, the start vertical signals STV1 and STV2 are generated according to the data clock signal CPV (see Figs. 3 and 4, for example).

In the present invention, the method according to claim 1 comprises the steps of receiving a vertical synchronizing signal. The vertical synchronizing signal is used as a reference basis. At the rising edge or the falling edge of the vertical synchronizing

signal, signals are processed to generate the control signals of the LCD module in real time. In DE mode (as disclosed in claim 6, for example), the data enable signal DE is first decoded to generate a vertical synchronizing signal. The vertical synchronizing signal is also used as a reference basis. At the rising edge or the falling edge of the vertical synchronizing signal, signals are processed to generate the control signals of the LCD module 10 in real time. Thus, a real time process rather than a cycle memory value is provided by the present invention, providing a real time process, to process control signals in real time, thereby acquiring a correct control waveform to drive the LCD module.

Furthermore, comparing the claimed features of the present application with the Applicants' admitted prior art, the Applicants' admitted prior art does not disclose pausing output of CPV, STV, and OE until the end of the vertical blank period VB. The Applicants' admitted prior art teaches only that, in a vertical blank period VB (v-blank) of the data enable signal DE, the start vertical signals STV1 and STV2 are generated.

In view of the foregoing amendments and remarks, it is respectfully submitted that the method of processing signals of a timing controller of a liquid crystal display device disclosed in independent claims 1 and 6 of the present application, as well as their dependent claims, is neither taught nor suggested by the prior art utilized by the Examiner. Accordingly, reconsideration and withdrawal of all objections and rejections are respectfully requested.

Favorable reconsideration and an early Notice of Allowance are earnestly solicited.

Because the additional prior art cited by the Examiner has been included merely to show the state of the prior art and has not been utilized to reject the claims, no further comments concerning these documents are considered necessary at this time.

CONCLUSION

In the event that any outstanding matters remain in this application, the Examiner is invited to contact the undersigned at (703) 205-8000 in the Washington, D.C. area.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

BIRCH, STEWART, KOLASCH & BIRCH, LLP

By _____
Joe McKinney Muncy, #32,334

P.O. Box 747
Falls Church, VA 22040-0747
(703) 205-8000

KM/asc

Attachments

OK to enter
LS 07.11.03

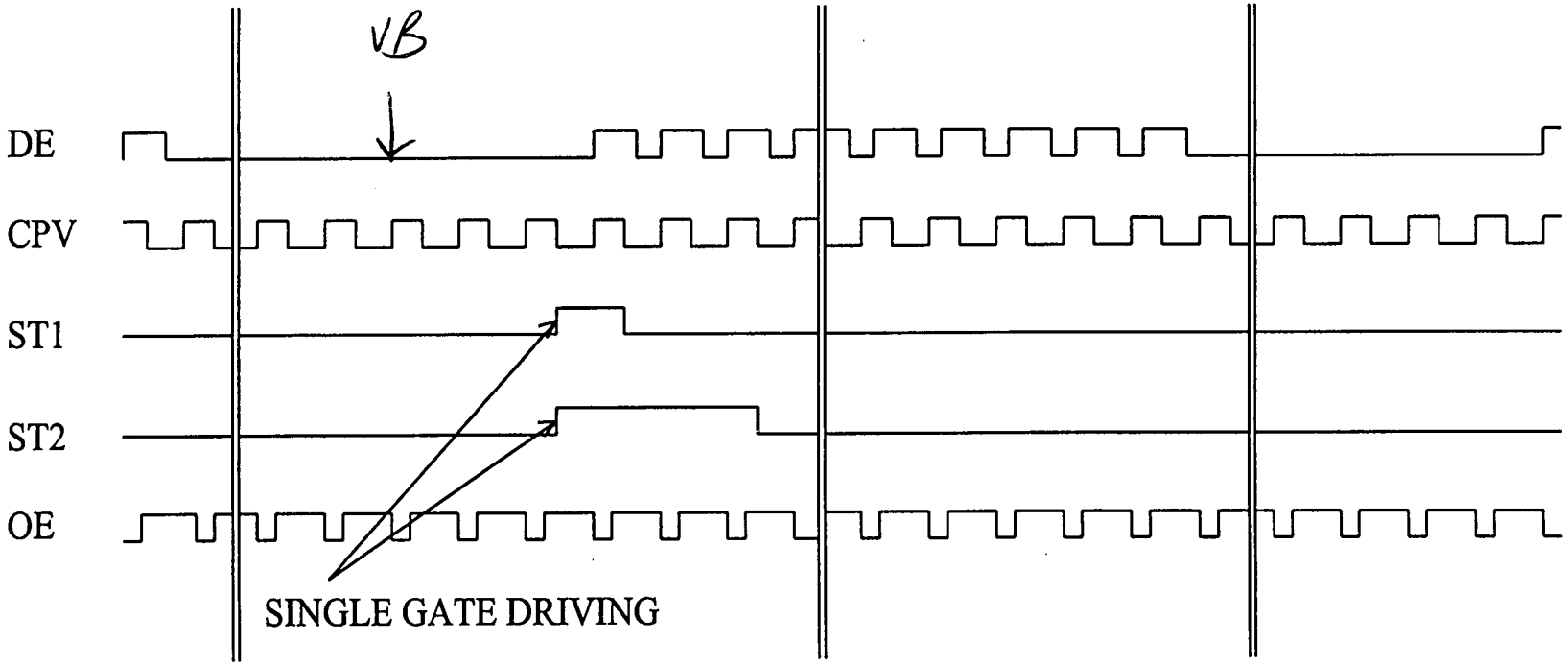

FIG. 4 (PRIOR ART)

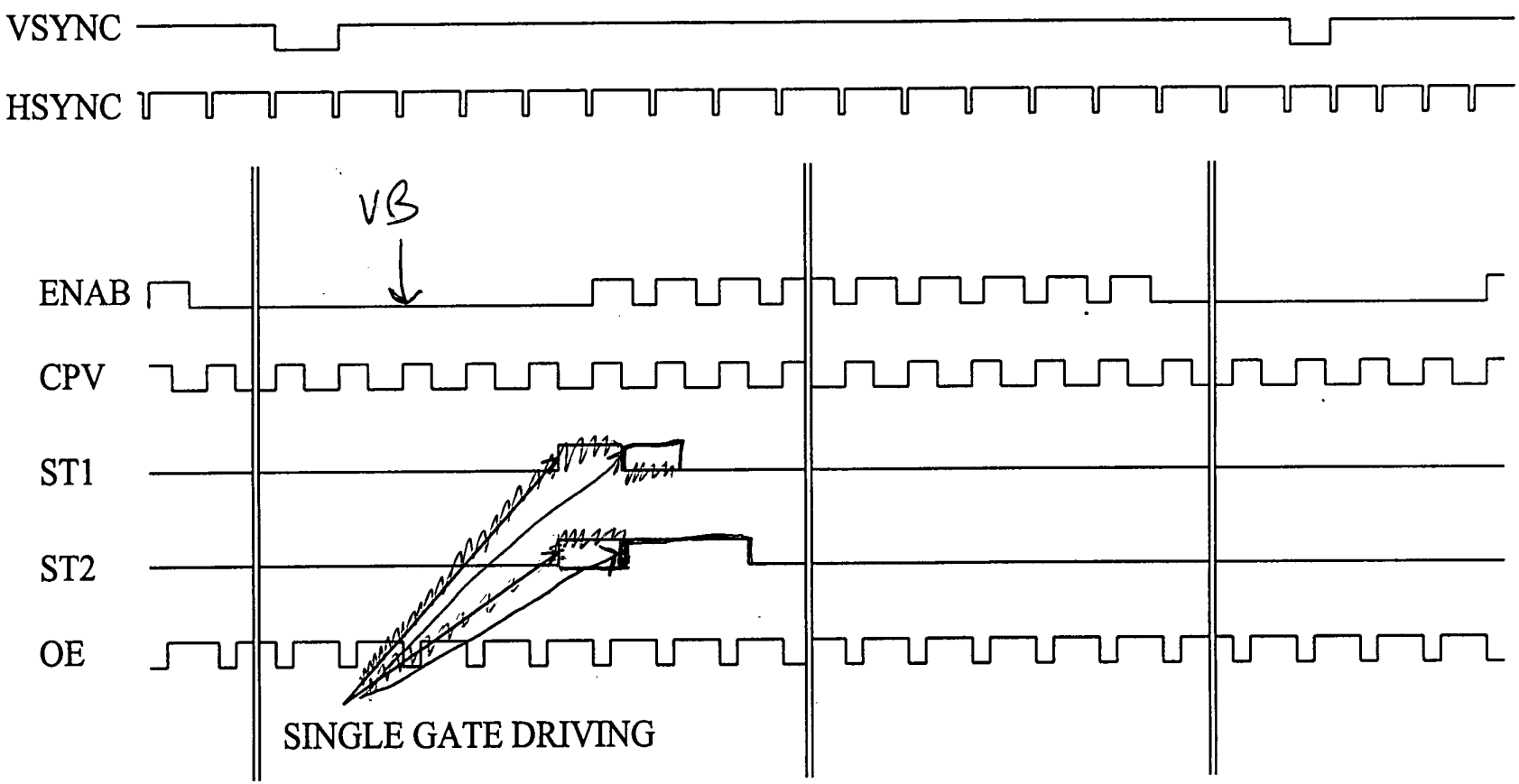

FIG. 5 (PRIOR ART)

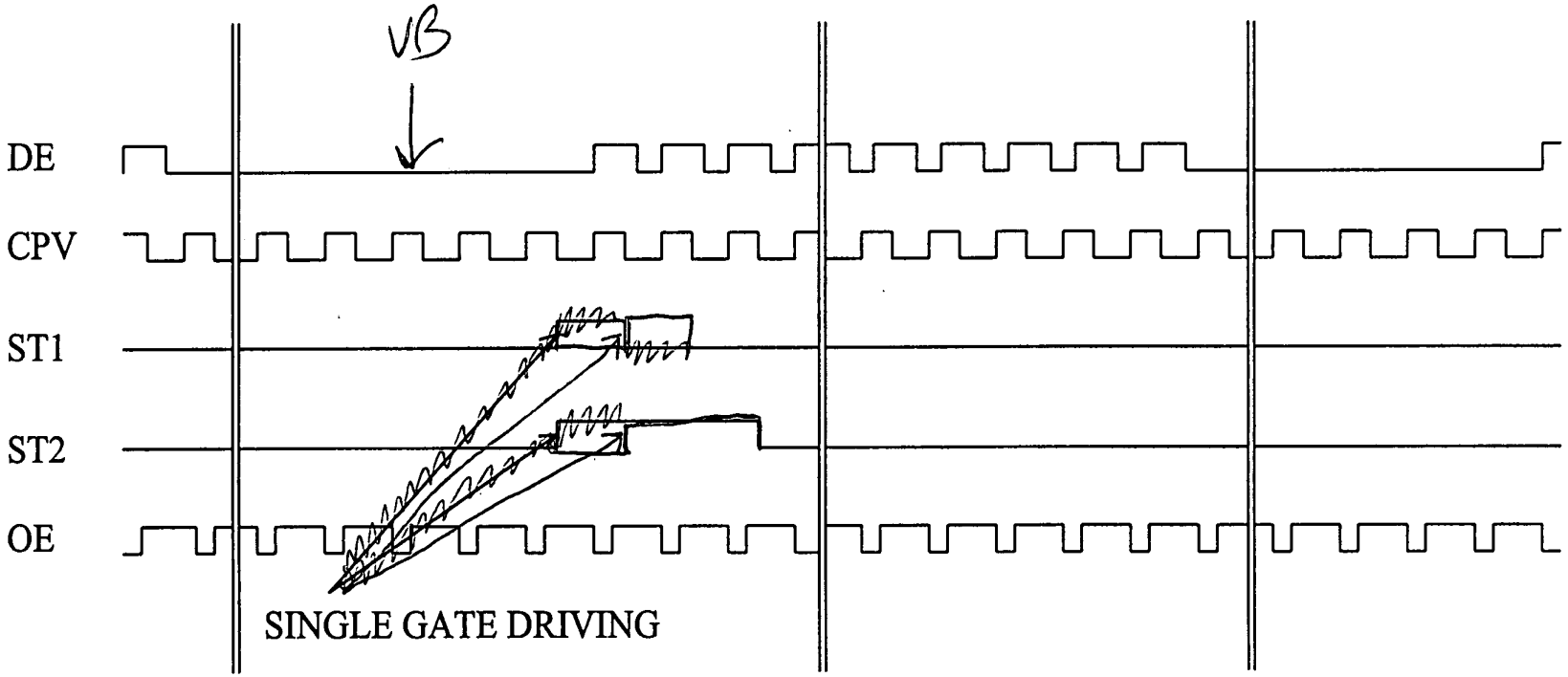

FIG. 6 (PRIOR ART)

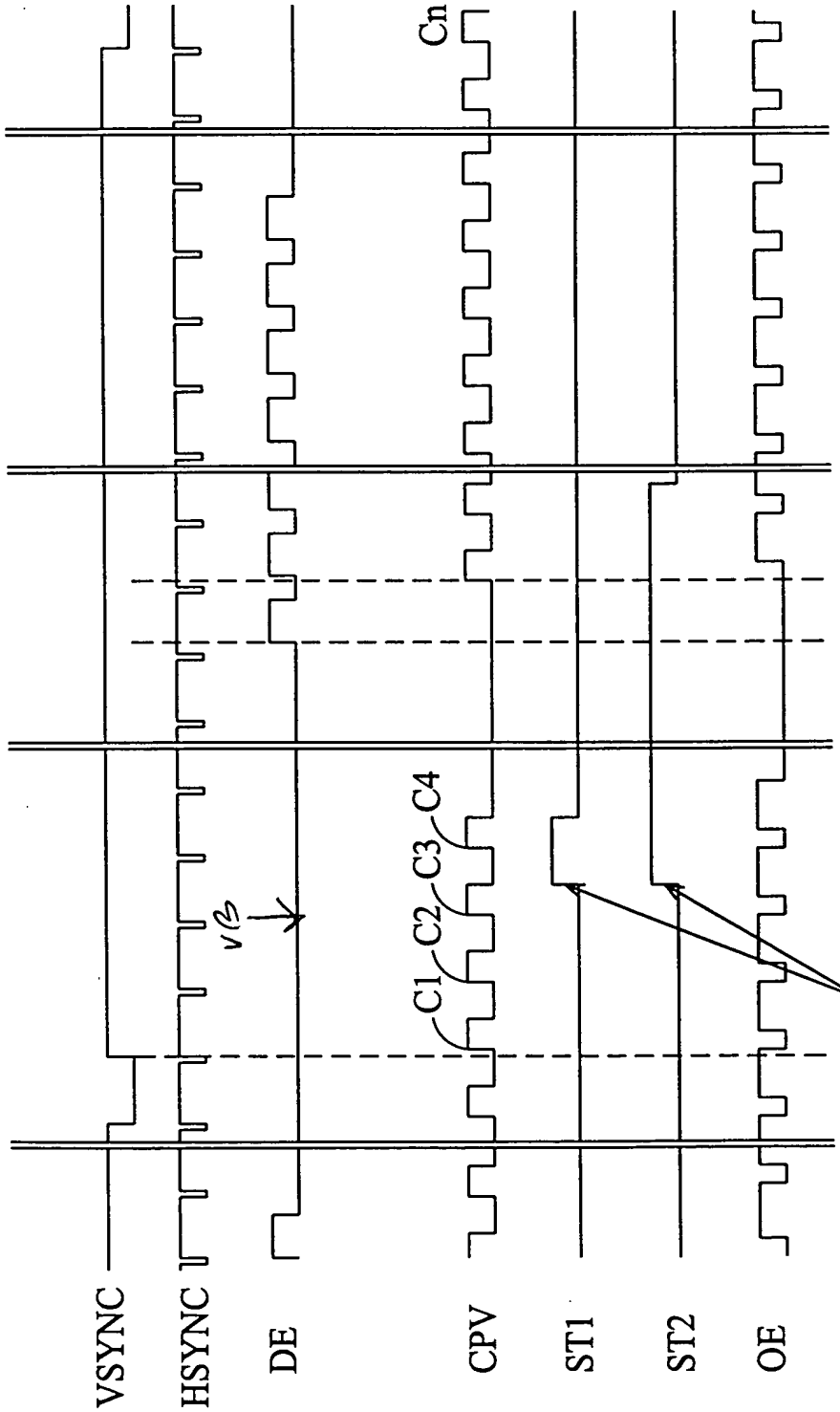

FIG. 7

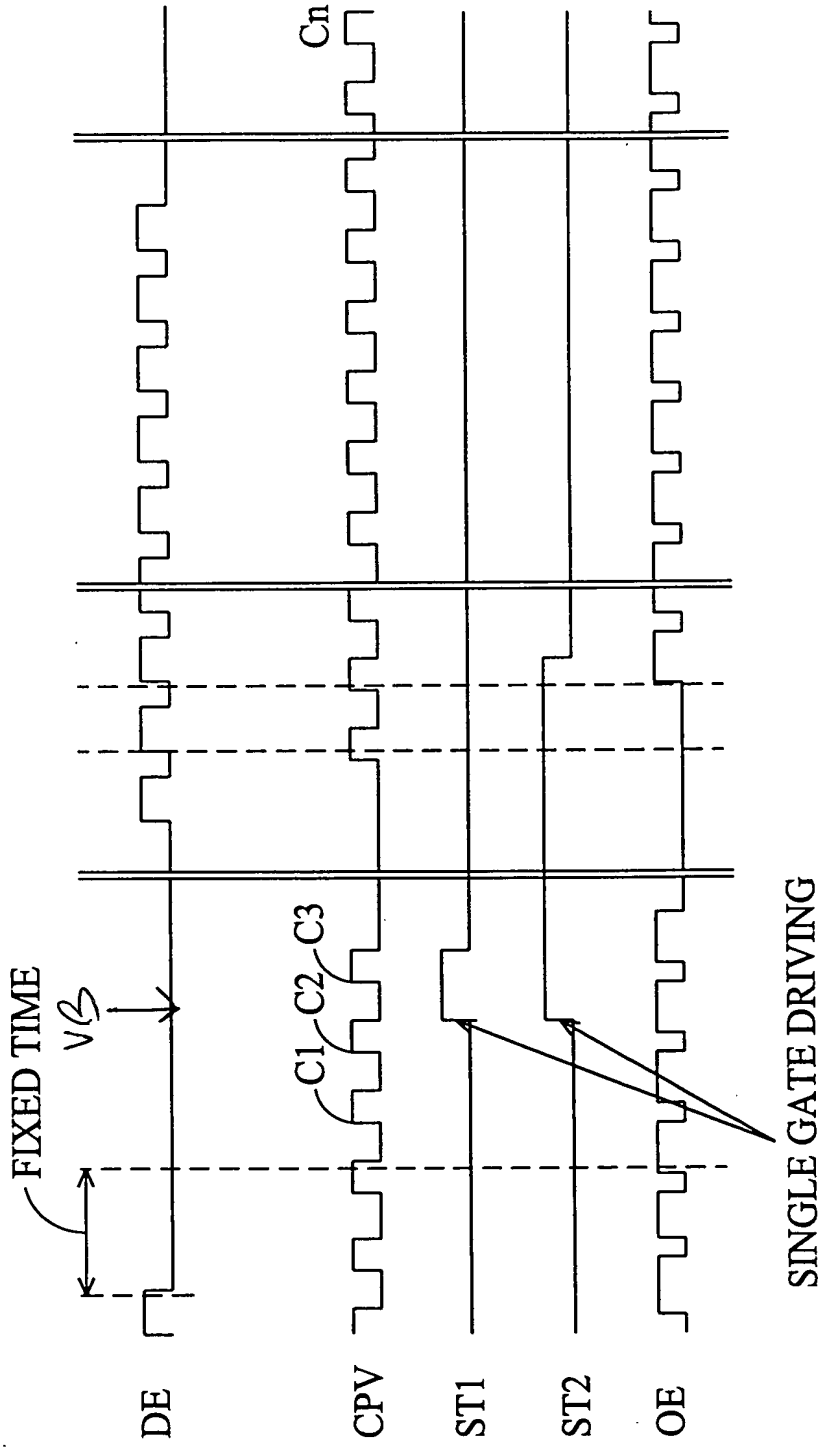

FIG. 8